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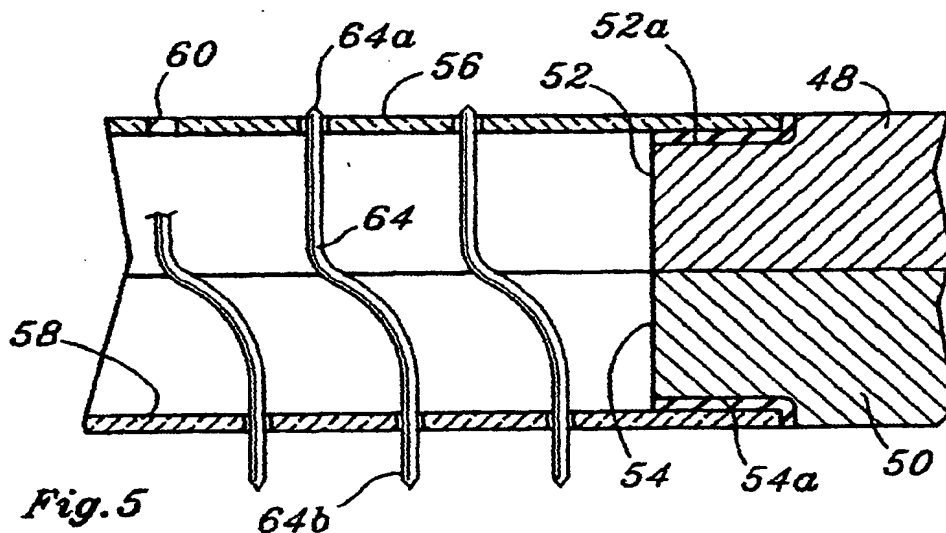
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(54) Title: TEMPERATURE COMPENSATED VERTICAL PIN PROBING DEVICE



(57) Abstract: An improved vertical pin probing device is constructed with a housing with spaced upper (48) and lower (50) spacers of Invar®, each having a thin sheet of silicon nitride ceramic material (56, 58) held in a window in the spacer by adhesive. The sheets of silicon nitride have laser-drilled matching patterns of holes (60) supporting probe pins (64) and insulating the probe pins from the housing. The Invar spacers and silicon nitride ceramic sheets have coefficients of thermal expansion closely matching that of the silicon chip being probed, so that the probing device compensates for temperature variations over a large range of probing temperatures.

TEMPERATURE COMPENSATED VERTICAL PIN PROBING DEVICE

TECHNICAL FIELD

This invention relates to an improved temperature compensated
5 vertical pin probing device for probing integrated circuits over a large
temperature range.

BACKGROUND ART

Integrated circuits in their wafer state are tested using probing devices,
the probes of which are traditionally of cantilevered or vertical configuration.
10 In a known type of vertical pin probing device, the probes are held between
spaced upper and lower dies and are generally curved with a straight portion
that protrudes substantially perpendicular through the lower die of the
housing. As the wafer under test is raised into contact with the probing
device, and then overdriven a few thousandths of an inch, the probes recede
15 into the housing, and the curved portion of the probe deflects causing spring
force that provides good electrical contact with the integrated circuit pads.

Traditionally, the housing is made from a dielectric material, often a
plastic such as Delrin®, trademark of E.I. duPont de Nemours & Co.

When a certain IC (integrated circuit) is tested at two or more
20 temperatures, over a large temperature range, for example 32 degrees F, room
temperature, and 275 degrees F, the typical prior art probe housing expands
with a significantly higher thermal expansion rate than that of the silicon
base material of the IC wafer under test. Such expansion causes a mismatch
of the probe locations and the IC pad locations, a condition that not only
25 results in failure to make satisfactory electrical contact, but may result in
fatal damage to the IC due to probe penetration in the circuit region of the IC.

One solution to this problem is to dimensionally compensate the room
temperature pitch dimensions of probes in the housing so that at the specified

test temperature it will have expanded to provide a nearly exact match of probe and pad positions. Except for temperatures within a narrow range, this option requires separate probe devices for each specific temperature, thus greatly increasing the user's monetary investment in probe devices.

5 Another solution would be to find a plastic or other suitable dielectric that matches the coefficient of thermal expansion of the silicon wafer. To date, however, the most practical choices of dielectric materials have expansion rates much higher than silicon. Plastics generally have a limited high temperature capability, thereby preventing their uses for high
10 temperature probing of IC's.

 One suggestion for temperature compensation of a vertical pin probing device is disclosed in co-pending application Serial Number 09/228,017 filed January 11, 1999 in the names of W. Thiessen and A. Evans and assigned to the present assignee. That application suggested a probe comprising a pair of
15 spacer members of Invar metal alloy, which has a coefficient of thermal expansion roughly equivalent to that of the silicon chip being probed. The spacer members had recesses supporting opposed channel-shaped insulating inserts of Vespel resin or Macor ceramic. The Macor ceramic had a coefficient of thermal expansion significantly greater than that of the silicon chip, and
20 required an anti-stick coating to provide the requisite lubricity to allow the probe pins to slide in the holes in the inserts. The assembly of the channel members in the recesses and subsequent drilling of the probe pin holes was a cumbersome process.

 Another suggestion is disclosed in co-pending application Serial
25 Number 09/228,016 filed January 11, 1999 and also assigned to the present assignee. That application disclosed foils of Invar used to support the probe pins in the Invar spacers, which have a coefficient of thermal expansion more closely matching that of the silicon. However, the foils are conductive and require an insulating coating to provide electrical insulation and lubricity.

30 It would be desirable to have a probe with all components more closely

matching the coefficient of thermal expansion of the silicon chip, which is simple and easy to construct, does not require added coatings and which is suitable for high temperature probing and probing over a large temperature range.

5 Accordingly, one object of the present invention is to provide a temperature compensated vertical pin probing device for probing integrated circuits over a large temperature range.

 Another object of the invention is to provide a vertical pin probing device which does not require application of special coatings to insulate or
10 provide lubricity.

 Another object of the invention is to provide an improved vertical pin probing device suitable for probing integrated circuits at very high temperatures, which is simple to construct.

DISCLOSURE OF INVENTION

15 Briefly stated, the invention comprises an improved temperature compensated vertical pin probing device for probing integrated circuits over a large temperature range, the integrated circuits having spaced contact pads on a circuit substrate to be contacted by probe pins for testing, the probing device being of a known type comprising upper and lower dies respectively
20 defining upper and lower patterns of holes therethrough corresponding to the integrated circuit contact pad spacing at a preselected temperature, and a plurality of probe pins, each pin being disposed in a pair of upper and lower holes and extending beyond the lower die to terminate in a probe tip, the improvement comprising a die member comprising a spacer member with a
25 coefficient of thermal expansion substantially matching that of the circuit substrate, said spacer member defining an aperture, a thin sheet of ceramic material disposed in said aperture with a coefficient of thermal expansion substantially matching that of the substrate, an adhesive securing the sheet of ceramic material in the aperture, the ceramic sheet defining a plurality of

holes therethrough forming one of said upper and lower patterns of holes.
Preferably the ceramic material is silicon nitride.

BRIEF DESCRIPTION OF DRAWINGS

The subject matter, which is regarded as the invention, is particularly
5 pointed out and distinctly claimed in the concluding portion of the
specification. The invention, however, both as to organization and method of
practice, together with further objects and advantages thereof, may best be
understood by reference to the following description, taken in connection with
the accompanying drawings, in which:

10 FIG. 1 is an elevational drawing in cross section showing a prior art
vertical pin probing device, together with portions of a printed circuit test
board and wired interface and portions of a silicon wafer and chuck support,

FIG. 2 is an enlarged side elevational view in cross section showing
15 details of the FIG. 1 prior art vertical pin probing device construction for two
probe pins,

FIG. 3 is a perspective view of the improved vertical pin probing device
according to the present invention,

FIG. 4 is a perspective view showing a cross section through the probing
device, taken along lines A-A of FIG. 3, and

20 FIG. 5 is an enlarged and exploded side elevational view in cross section
illustrating portions of the probing device of FIGS. 3 and 4.

DETAILED DESCRIPTION OF THE DRAWINGS

Before describing the improvements of the present invention, reference
should be made to FIGS. 1 and 2 of the drawing illustrating a prior art vertical
25 pin probing device used with an interconnecting device called a "space
transformer" and a printed circuit board. The simplified view of FIG.
1 illustrates a prior art construction. A printed circuit test board 10
sometimes called a "probe card" includes conductive traces 12 which are

connected in test circuit relationship to integrated circuit test equipment (not shown). In practice, the traces 12 lead to "pogo pads" on the printed circuit board, to which the external test equipment leads are connected in a prescribed test. An integrated circuit 14 or other device under test is supported on a movable chuck 16. Integrated circuit 14 typically has a pattern or matrix of contact pads to be simultaneously probed by a vertical-pin integrated circuit probing device 18, such as the COBRA® probe head sold by Wentworth Laboratories. Probing device 18 includes a lower die 20 with a group of holes 21 and upper die 22 with a group of holes 23 separated by a spacer 24 and carrying multiple vertical pin probes 26, 28. The die materials are typically made of a plastic insulating material such as Delrin®, an acetyl resin manufactured by E.I. duPont de Nemours & Co.

Reference to the enlarged cross-section view FIG. 2 illustrates that the two representative probes 26, 28 include probe tips 26a, 28a respectively protruding from holes 21 in the lower face of lower die 20 and exposed heads 26b, 28b respectively protruding from holes 23 in the upper side of upper die 22. The holes 21, 23 containing the opposite ends of the vertical probe pins 26, 28 are slightly offset from one another and the probe pins are curved in a snake-like configuration to promote buckling, so as to create substantially uniform contact pressure on the integrated circuit pads 14a, 14b despite any slight vertical unevenness or misalignment.

A prior art space transformer shown in FIG. 1 is indicated generally at 29 and comprises a mounting block 30 with a well 32 formed therein. At the bottom of the well, a number of holes 34 are laid out to dimensionally correspond to a first small inner pattern defined by the exposed heads 26b of the probe head assembly 18. The probing assembly 18 is shown separated from the space transformer 29 for clarity but is connected thereto in actual operation by screws (not shown).

An individual insulated wire 36 is connected to PCB trace 12 at one end and on the other end, the wire extends into a hole 34 in the mounting block 30

so as to be in electrical contact with probe head **26b** on the underside of block **30** when the probe assembly **18** is bolted to the space transformer **29**. A similar wire **37** cooperates with probe head **28b**.

Space transformer **29** is attached to the PC board by means such as screws **38**, and an epoxy potting compound **39** immobilizes wires **36**, **37**. The probing device **18** is attached to the underside of space transformer **29** by screws (not shown), so that probe heads **26b**, **28b** make electrical contact with leads **36**, **37**. The integrated circuit **14** has a number of spaced contact pads, such as **14a**, **14b**, spaced apart by dimension **A**. The probe tips **26a**, **26b** are spaced apart by dimension **B**. Prior art devices in which the coefficient of thermal expansion of the die material is substantially different from the coefficient of thermal expansion of the silicon wafer (.00000156 inches per inch per degree F or .0000028 meters per meter per degree Kelvin) will result in a mismatch between dimensions **A** and **B** to a degree which depends on the temperature range of probing.

BEST MODE FOR CARRYING OUT THE INVENTION

Referring now to FIGS. 3, 4 and 5 of the drawing, the improved temperature compensated vertical pin probing device is indicated generally by reference numeral **40** and comprises an upper die member **42** and a lower die member **44**. The dies are held together and mounted to the mounting block **30** shown in FIG. 1 by means of screws (not shown) passing through suitably placed holes **46** around the perimeter. Each of the upper and lower die members includes a spacer member **48**, **50** respectively with a rectangular aperture **52**, **54** respectively. Each aperture **52**, **54** holds a thin ceramic sheet **56**, **58** respectively. The spacer members **48**, **50** are fabricated from a substrate core material having a coefficient of thermal expansion as close as possible to that of the silicon making up the circuit substrate. One preferred material is a nickel metal alloy of Invar®, (registered trademark of Imphy S.A.) having a coefficient of thermal expansion of .00000100 inches per inch

per degree F (or .0000018 meters per meter per degree Kelvin) at a nominal composition of 36% nickel, which is slightly less than that of silicon. The thermal coefficient of expansion may be varied so as to coincide exactly with that of silicon, if desired, by adjusting the percentage of nickel in the alloy as known in the art. (Sisco, Modern Metallurgy for Engineers, 2nd Edition, p. 299).

As previously known in the art, probe pins 64 extend between the pattern of spaced and offset holes 60, 62 in the upper and lower die members respectively. The upper ends of the probe pins 64 terminate in probe tips 64a which are disposed and make electrical contact with the wires such as 37 (FIG. 1) leading to the printed circuit test board. The lower ends of the probe pins 64 terminate in probe tips 64b which slide in holes 62 in known manner during probing of wafer 14 (FIG. 1).

Referring to the cross section of Fig. 4 taken along lines A-AF Fig. 3, it is seen that the periphery of the upper ceramic sheet 56 is mounted adjacent the upper surface of spacer member 48 and the lower ceramic sheet 58 is mounted in a peripheral frame adjacent the lower surface of spacer member 50, so that the two ceramic sheets are held apart in spaced relationship. The upper ceramic sheet 56 contains a plurality of holes 60 drilled by laser in a predetermined pattern. The lower ceramic sheet contains a plurality of holes 62 similarly drilled by laser in the same predetermined pattern, except that the pattern is offset from the upper pattern in the plane of the ceramic sheet. This provides pairs of holes which are laterally offset from one another.

Reference to the enlarged cross sectional drawing of Fig. 5, which is not to scale, illustrates a portion of the probe assembly 40. Aperture 52 in spacer 48 is enlarged about its periphery in the upper face to provide a ledge 52a, and a similar peripheral ledge 54a is provided in the lower face of spacer member 50. The upper ceramic sheet 56 is relatively thin (10 mils) and the lower ceramic sheet is also relatively thin, but thicker than the upper sheet, having a preferred dimension of about 20 mils in thickness. The ceramic

sheets 56, 58 are restrainably mounted within the openings on ledges 52a, 54a respectively by means of a high strength rigid adhesive such as epoxy.

In accordance with the present invention, we have discovered that silicon nitride ceramic is ideally suited for the ceramic sheets used in the improved vertical pin probing device. Silicon nitride ceramics offer high mechanical strength at elevated temperatures, thermal shock resistance and toughness as well as having a low coefficient of friction to enable sliding of the probe pins without the necessity of a coating of anti-stick material. The silicon nitride sheet is normally produced by hot pressing and is a two phase, alpha and beta, polycrystalline ceramic. It has a coefficient of thermal expansion of 1.7×10^{-6} inches per inch per degree F (or .0000034 meters per meter per degree Kelvin), which is only slightly greater than the coefficient of thermal expansion of silicon. Since the thermal coefficient of the spacer member is slightly less than that of silicon and the thermal coefficient of silicon nitride is slightly greater than that of silicon, the two materials used in the die member cooperate with one another to cause the overall thermal coefficient of the die member to closely approximate that of the silicon wafer.

INDUSTRIAL APPLICABILITY

The operation of the invention may be described as follows. Since the Invar material has a coefficient of thermal expansion slightly lower than, but substantially matching, that of the silicon, the Invar upper and lower dies expand substantially so as to dimensionally correspond to the expansion of the silicon wafer. Therefore the location of the centerlines of ceramic sheets 56, 58 and holes 60, 62 are located in accordance with the contact pads on the silicon wafer, and follow the expansion and contraction of the silicon wafer.

The ceramic sheets 56, 58 may expand and contract about their own centerlines with a slightly higher coefficient of thermal expansion than the silicon wafer and the spacer members 48, 50. However, the inserts are restrained by the adhesive and only permitted to expand in a direction

perpendicular to the plane of the wafer. Therefore, despite the fact that the coefficient of thermal expansion of the insulated inserts may be slightly higher than that of the silicon wafer, it does not cause any significant mismatch between wafer contact pads and probe points over a large temperature range.

5 The lubricity provided by the preferred ceramic material allows the probe pins to slide without requiring an anti-stick coating.

While there has been described what is considered to be the preferred embodiment of the invention and one modification thereof, other modifications will occur to those skilled in the art, and it is desired to secure in the

10 appended claims all such modifications as fall within the true spirit and scope of the invention.

CLAIMS

1. An improved temperature compensated vertical pin probing device for probing integrated circuits over a large temperature range, the integrated circuits having spaced contact pads on a circuit substrate to be contacted by probe pins for testing, the probing device being of a known type comprising upper and lower spaced die members respectively defining upper and lower patterns of holes therethrough corresponding to the integrated circuit contact pad spacing at a preselected temperature, and a plurality of probe pins, each pin being disposed in a pair of upper and lower holes and extending beyond the lower die to terminate in a probe tip, the improvement comprising a die member having a spacer member with a coefficient of thermal expansion substantially matching that of the circuit substrate, said spacer member defining an aperture therethrough, a thin sheet of ceramic material disposed in said aperture with a coefficient of thermal expansion substantially matching that of the circuit substrate, and an adhesive securing the sheet of ceramic material in said aperture, said insert defining a plurality of holes therethrough forming one of said upper and low patterns of holes.

2. The improvement according to Claim 1, wherein the coefficients of thermal expansion of the spacer member and the sheet of ceramic material are respectively slightly lower than and slightly higher than the coefficient of thermal expansion of silicon.

3. The improvement according to Claim 2, wherein said spacer member is of Invar metal alloy.

4. The improvement according to Claim 2, wherein said ceramic sheet is silicon nitride.

5. The improvement according to Claim 1, wherein the spacer member has a surface surrounding the aperture and wherein the aperture defines a peripheral ledge adjacent the surface, said sheet of ceramic material having a periphery disposed on said peripheral ledge.

6. The improvement according to Claim 5, wherein the adhesive is epoxy resin and secures the periphery of the sheet of ceramic material to said peripheral ledge.

5 7. The improvement according to Claim 1, wherein the spacer member is of Invar metal alloy, the sheet of ceramic material is of silicon nitride, and the adhesive is of epoxy resin.

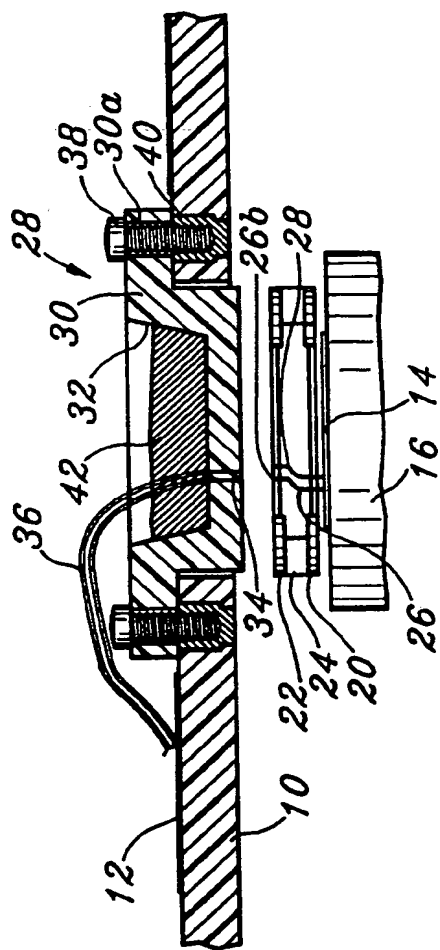


Fig. 1
Prior Art

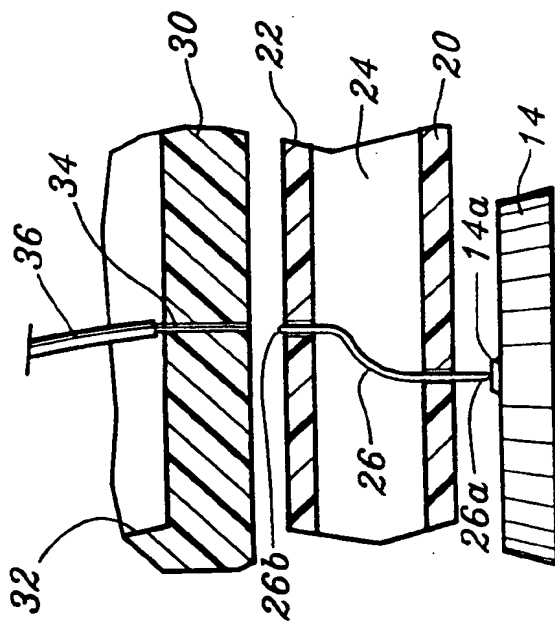


Fig. 2
Prior Art

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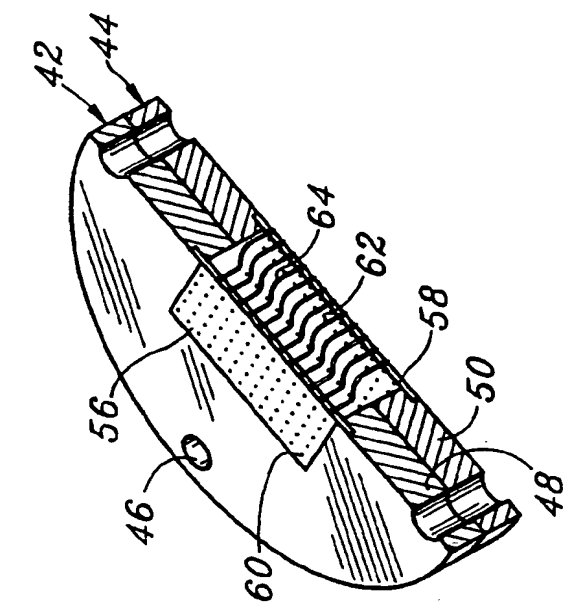


Fig. 4

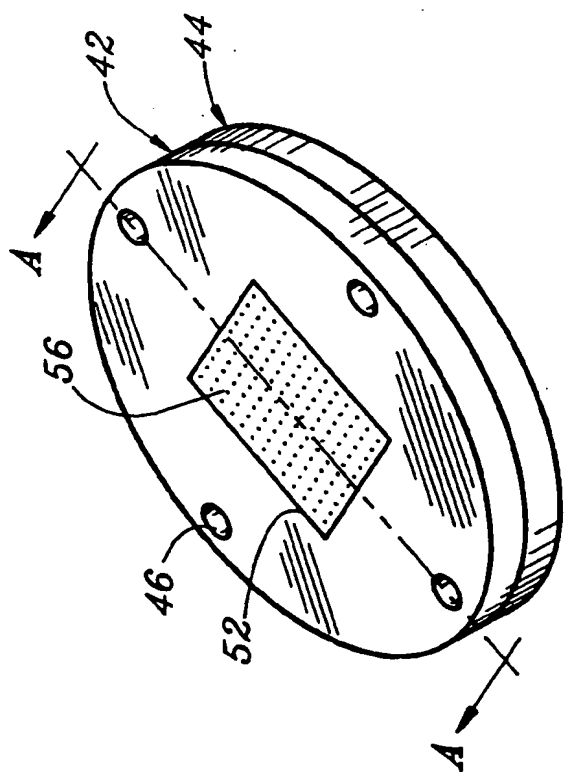


Fig. 3

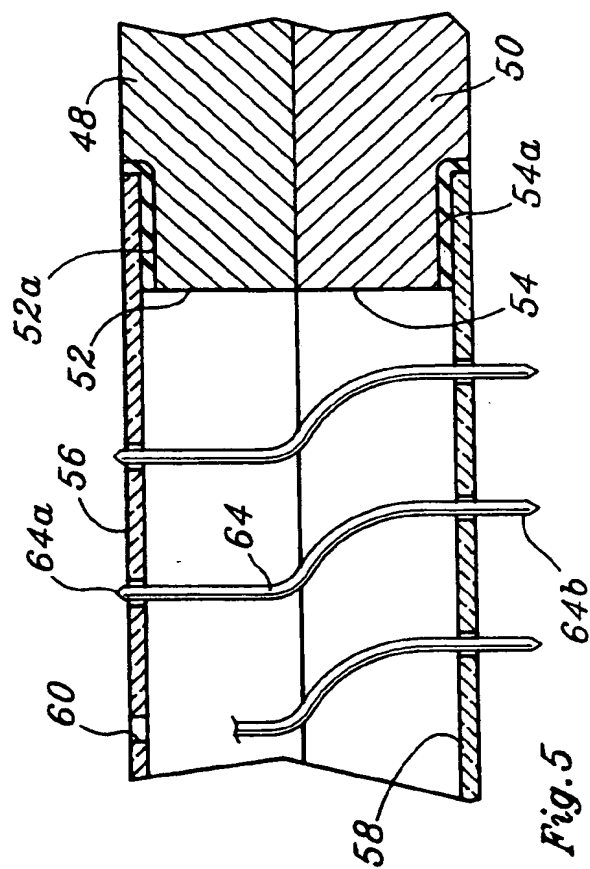


Fig. 5